ABSTRACT

The present invention discloses a processor system comprising a processor (31) and at least a first memory (32) and a second memory (34, 36, 37). The first memory (32) is normally faster than the second one, and means for memory allocation (38, 41, 48) perform the periodically static allocation of data into the first memory (32). The means for memory allocation (38, 41, 48) are run-time updateable by software. An execution profiling section (39) is provided for continuously or intermittently providing execution data used for updating the means for memory allocation (38, 41, 48). According to the invention, the memory allocation is performed on a variable or record (49, 50) level. The means for memory allocation preferably use linking tables (41, 48) supporting dynamic software changes. The first memory (32) is preferably an SRAM, connected to the processor by a dedicated bus (33).

(Fig. 2)